C-Element Metastability Mitigation using Schmitt-Trigger

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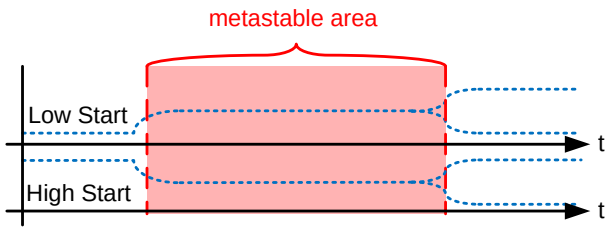

Figure 1. Metastability behavior of a storage loop (inverting node)

I. The Problem

As all state holding elements, Muller C-elements are prone to metastable upsets [1], [2], [3]. In case of an input spike or a short overlap of both input signals, a metastable state may arise in the element. The cause for the problem is that the storage loop starts to flip its state but while doing so, the input is removed and the loop is left in an undecided state. Based only on the characteristics of the loop, the resolution process may take an arbitrary long time. The outcome of the resolving process can either be a flip of the state, or the state my not change after all.

Figure 1 shows the typical behavior of a metastable logic gate. It can be seen that the storage loop starts to change its value but then enters the metastable region and does not leave it for an extended time. The resolution may be either of the both stable states.

While the resolving process is active, the nodes of the storage loop are at intermediate, analog voltage levels [2]. The voltage levels as well as the metastable response may be estimated using a Spice analysis [4].

As has been previously shown [5], metastability is unavoidable. Therefore one can not hope to devise a functioning countermeasure eliminating metastability. It may nevertheless be possible to mitigate or convert the malicious effects of metastability into a more benign form. This conversion is even more essential as metastability may fool conventional error containment circuits (like voters, e.g.) [6].

Such a containment is especially important for asynchronous circuits. In contrast to synchronous circuits no temporal masking is present, meaning that the asynchronous circuit may propagate the erroneous state immediately, whereas the propagation in synchronous circuits is only done at clock edges. Therefore it is unacceptable to generate even short analog output values or output pulses.

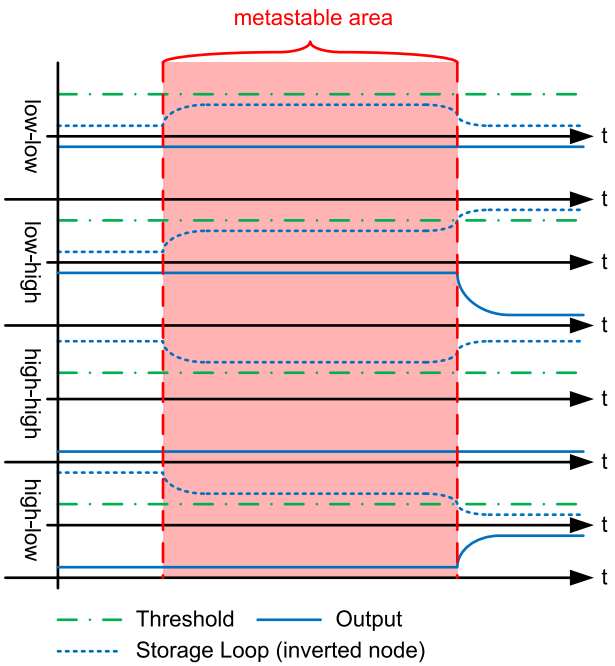

Figure 2. Metastability mitigation principle

II. Proposed Solution

To circumvent the malicious effects of metastability, we want to present a solution which is capable of converting any metastable state into a late transition, if the state is eventually flipped, or suppresses any output change, if the state is not changed. To be able to achieve this goal, the output may only change after the outcome of the metastability resolution process is definite. From Figure 1 it is apparent that this is only true, after the metastable state is completely resolved. For the upper case in the figure this means that the voltage of the inverting storage loop node must rise significantly above the metastable voltage while for the lower case, the voltage must fall below it. Therefore, dependent on the initial state of the element, an adaptive threshold is required.

Figure 2 illustrates the idea of the solution. The adaptive threshold must always be on the opposite side of the metastable voltage (as far as the inverting loop node is concerned). Only after metastability is resolved, this threshold

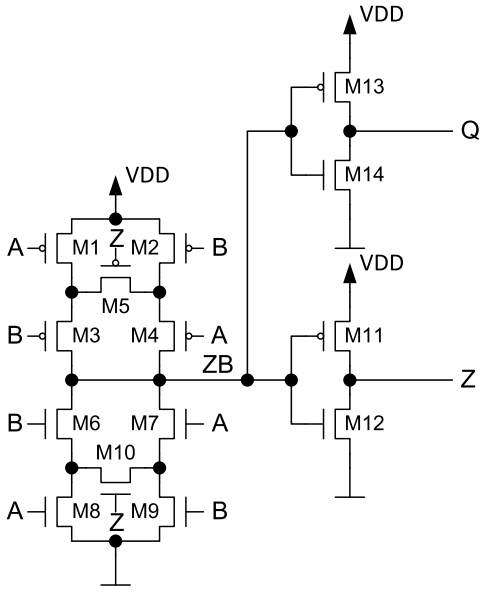

Figure 3. Van-Berkel Muller C-element CMOS implementation

is crossed and the output flipped. Such a behavior can be found in an inverting Schmitt-Trigger.

III. Experimental Validation

To show the correctness of the solution we modeled a van-Berkel Muller C-element (see Figure 3 for the circuit and [7] for details) using Spice. We used a single sizing for the circuit. The sizing confirms to the rules given in [7].

To verify the claim that an adaptive threshold securely converts the analog metastability voltage to a late transition, we devised a simulation environment. We simulate different overlap times, starting with a time that surely flips the state of the Muller C-element and another one that leaves the state unchanged. The differences in the overlap times are then divided by two and a new simulation with the resulting overlap is performed. If the new simulation flips the element's state, it is used as new upper bound, otherwise as new lower bound. This procedure is repeated as long as the numeric precision of the simulator allows. After the process is finished, the traces for the upper and lower bound are plotted.

The first simulation was performed using the standard van-Berkel implementation. As the output inverter (M13, M14) and the loop inverters have the same sizing, their threshold is the same and the analog metastability voltage is copied to the output (see Figure 4).

When simulating our proposed version (using the inverting Schmitt-Trigger output stage (see Figure 5 for the output driver circuit [8]), however, there is no analog voltage present at the output. Furthermore the output only changes after the metastable state has been resolved (see Figures 6 and 7). Therefore the metastable state is masked out or converted to a late transition in all possible cases.

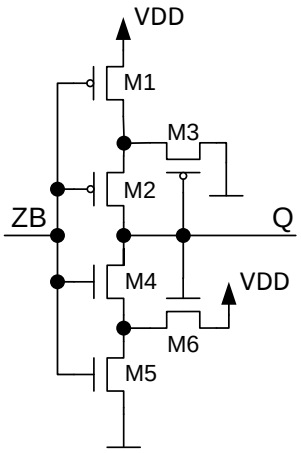

Figure 5. Schmitt Trigger CMOS circuit

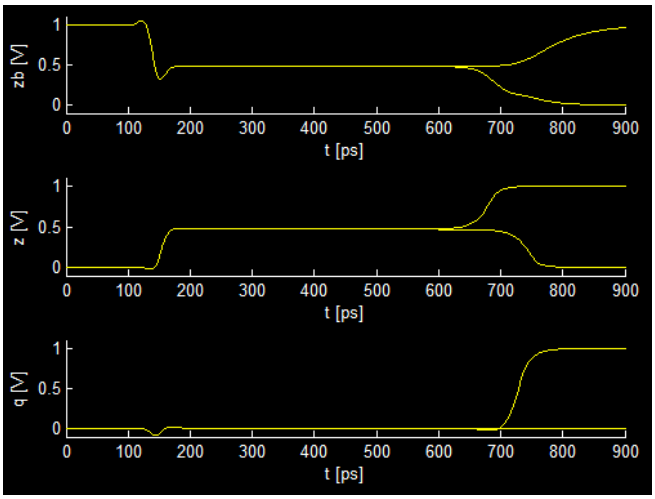

Figure 6. Simulation result for the van-Berkel implementation with the Schmitt-Trigger output stage (inverting loop node starting high)

IV. Limitations of the Approach

As was already shown by [5], a Schmitt Trigger output stage is counterproductive in case of synchronous circuits. The additional delay of the Schmitt Trigger in the fault free case costs too much of the overall resolution time and therefore increases the error rate instead of mitigating the effects of metastability. The root of the problem is that the resolution time is fixed by the static clock period in this case. In asynchronous circuits, however, the resolution time can be naturally stretched by the local handshaking protocol. Therefore we have always sufficient resolution time available, even with the added delay of the Schmitt Trigger.

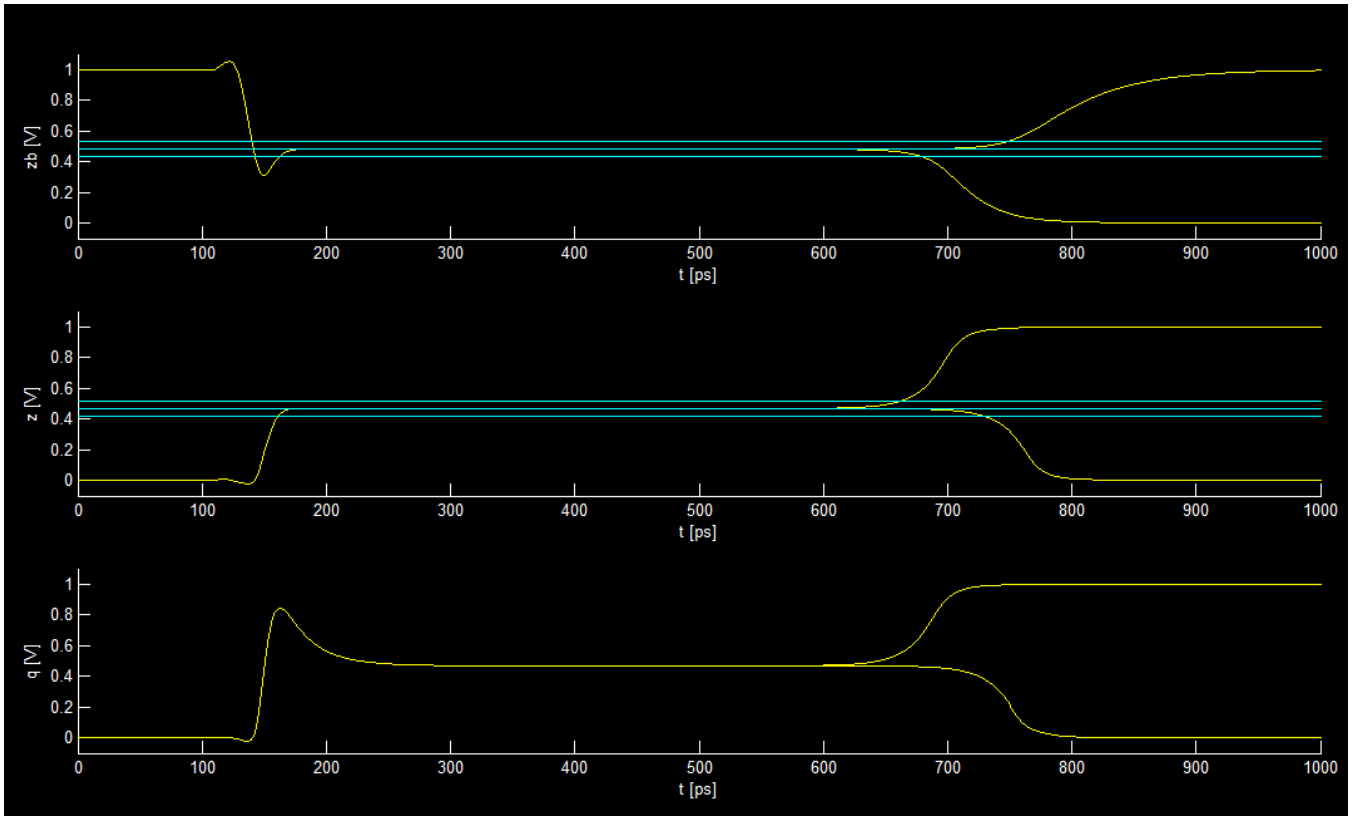

Figure 4. Simulation result for the standard van-Berkel implementation

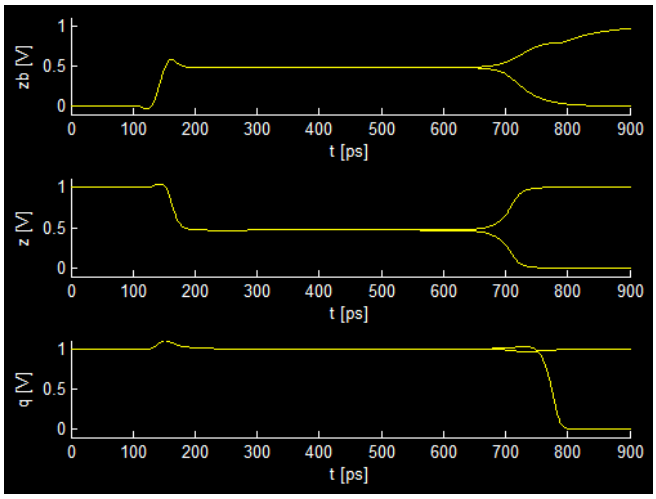

Figure 7. Simulation result for the van-Berkel implementation with the Schmitt-Trigger output stage (inverting loop node starting low)

V. Conclusion

A Schmitt Trigger output stage is able to securely convert the metastable voltage present in the storage loop into late transitions. The local handshake protocols of asynchronous circuits compensates the negative effects on the error rate Schmitt Triggers have in synchronous circuits.

This is a preliminary analysis of the topic. A more elaborate analysis of metastability mitigation in Muller C-elements will be published as conference paper soon.

References

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