Single Event Effect Measurements in 90nm CMOS Circuits at the Microbeam Facility for the Project FATAL*

M. Hofbauer[1,#], K. Schweiger[1], H. Dietrich[1], H. Zimmermann[1], U. Schmid[2], B. Merk[3], K.O. Voss[3]

[1]TU Wien, EMCE, Austria; [2]TU Wien, ECS, Austria; [3]GSI, Darmstadt, Germany

Introduction

Final goal of the project FATAL is a simulation model which considers radiation induced effects, like single event transients (SETs) and single event upsets (SEUs), in asynchronous logic. Using this model, it will be possible to develop a design and simulation framework for designing radiation tolerant asynchronous logic. For synchronous logic such frameworks are already available. Synchronous logic is sensitive to single event effects (SEEs) at the clock edge only. Therefore it is sufficient to know the arising pulse widths of the SETs in order to design radiation tolerant synchronous logic [1]. In asynchronous logic there is no clock available. Thus it is sensitive to SEEs all the time. Furthermore, handshaking and data signals work with voltage transitions. Since SETs are nothing else than voltage transitions they can easily be misinterpreted as data or handshaking signals. To consider single event effects in a simulation model for asynchronous logic, it is necessary to know the exact shape of the arising SETs and the propagation of these pulses through the circuitry.

Simulation

For investigation of SEEs, extensive 3D semiconductor simulations have been performed. The final simulation model will be significantly less complex in order to reduce the computational effort. This simplified model has to be verified by measurements and 3D semiconductor simulations that are very sensitive to process parameters like doping profiles. Therefore the 3D semiconductor simulations have to be calibrated with help of measurements. First measurements have been performed in 2011 at the micro-beam facility using 945-MeV gold ions.

Measurement

Simulation results showed a strong position dependency of SEEs. Therefore it is necessary to be able to accurately deposit the ions at the desired position. Furthermore, the effects of several ions should not overlap. According to this, the circuit should be hit by only one single ion at a time. These two requirements are perfectly met by the micro-beam facility at the UNILAC. It is able to deposit single ions in a region with a diameter of approximately 500nm. For measurement of the arising SETs and SEUs, test chips with integrated sense amplifiers have been designed and fabricated. These sense amplifiers allow measurement of the voltage transients with negligible influence on the test circuit and pulse shapes. Fig. 1 shows the measurement setup. The micro-beam scans the surface of the chip. Every time an ion hits the chip, the channeltron generates a signal which triggers the oscilloscope and forces the system control to log the position of the beam in order to correlate the hit position with the measured pulses. Basic logic circuits like inverter chains and Muller-C pipelines have been investigated. Muller-C Gates are basic memory elements for asynchronous logic. SETs and SEUs could be observed.

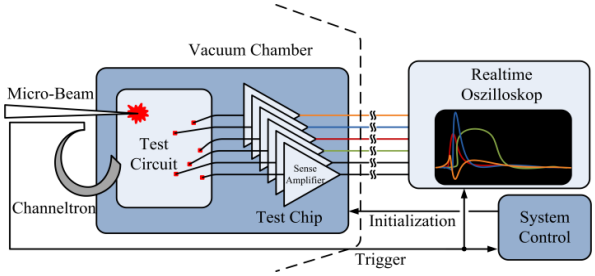

Figure 1: measurement setup

Results

Fig. 2 shows a voltage transient recorded in a single inverter. Using on chip sense amplifiers, it was possible for the first time to directly measure the voltage pulse shapes of SETs and SEUs. More detailed information is published in [2].

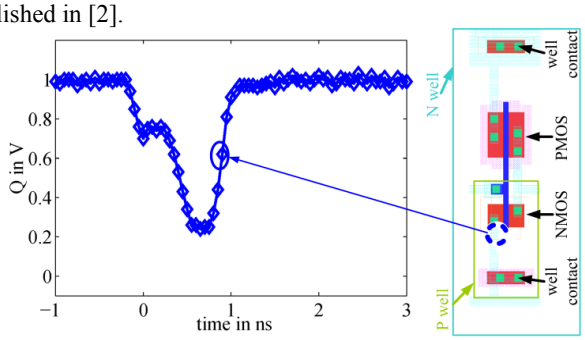

Figure 2: measurement result

References

[1] M. J. Gadlage et al., "Scaling Trends in SET Pulse Widths in Sub-100 nm Bulk CMOS Processes," IEEE Transactions on Nuclear Science, 57 (2010) 3336.

[2] K. Schweiger, M. Hofbauer et al, “Position Dependent Measurement of Single Event Transient Voltage Pulse Shapes under Heavy Ion Irradiation”, accepted in Electronics Letters.

* This research is supported by the Austrian Science Fund (FWF): P21694

Michael.Hofbauer@tuwien.ac.at